ABSTRACT OF THE DISCLOSURE

A manufacturing method of a semiconductor device in which the influence of alignment errors is decreased is provided. A semiconductor device includes a plurality of elements each having the same structure composed of a plurality of layers including the same plural patterns respectively. One-shot exposure is performed for forming patterns on layers on which the patterns are formed before the formation of a pattern on the layer including wiring substantially affecting the operation of the semiconductor device when the value of the parasitic capacitance generated according to a positional relationship between the wiring and other wiring is different between elements. Division exposure is performed for forming patterns on all of the other layers on which the patterns are formed after the one-shot exposure.